IN THE SPECIFICATION

Please replace the first full paragraph on page 7 with the following:

[0024] As will be evident to one of ordinary skill in the art, the principles of this invention are independent of the particular logic and structure of the activity detector 180 of FIG. 2. The function of the activity detector is to re-enable the bus interfaces 125 at each target 120 by the time that the control and data and commands arrive at the interfaces 125, and can be effected in any of a variety of means, and the function can be distributed among a variety of blocks. For example, each interface 125 could be configured to receive the system clock as a direct input, and the output of the gate 220 of FIG. 2 as an input. The gate ~~230~~ 220 in this example would then be located in each of the target interfaces 125. By providing an ungated system clock and a clock-gating signal to each interface 125, each interface 125 can be selectively configured to use the power-saving option of this invention for some or all of the components in the particular target interface 125. For example, the registers in a particular interface 125 that are used for receiving control signals may be configured to use the ungated system clock, while the registers that are used for communicating data and commands may be configured to use the gated clock output of the gate ~~230~~ 220 within the particular interface 125. In like manner, the enable-override gate 220 may be included in each target interface 125, so that each target 120 can be selectively placed in a low-power mode. If, for example, due to the particular placement of a target 120 in the layout of the system, the propagation delay of the clock-gating signal to the target 120 is excessive, this particular target 120 can be configured to forego the power-savings and remain in a continuous monitoring mode for more reliable operation. These and other system configuration and optimization options will be evident to one of ordinary skill in the art in view of this disclosure. For example, other components, such as select registers within the bus controller 150 may also be configured to be operated based on the clock-gating signal from the activity detector 180 to further reduce the power consumption of the system.